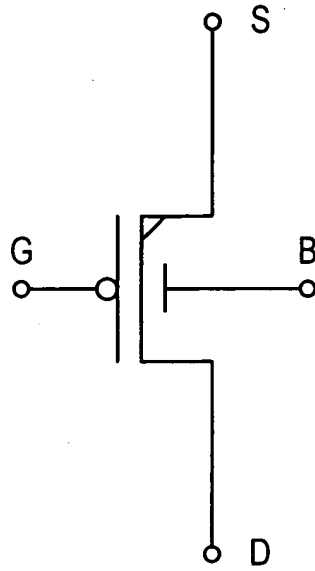
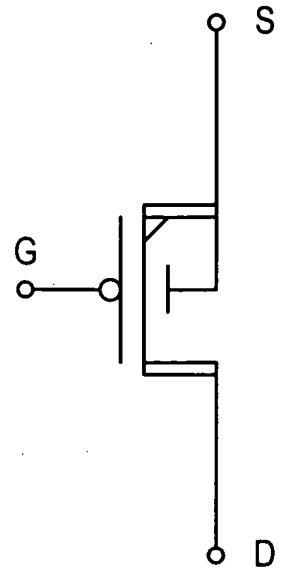


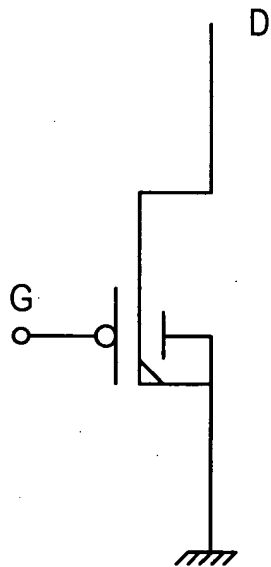
(a) 5V NMOS



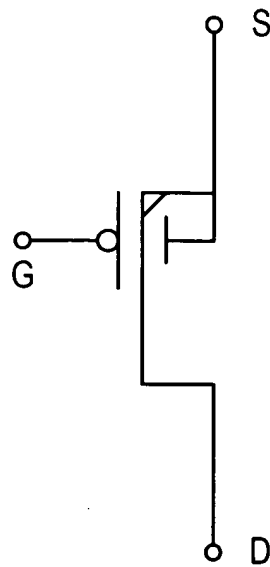
(b) 5V PMOS



(c) HV PMOS



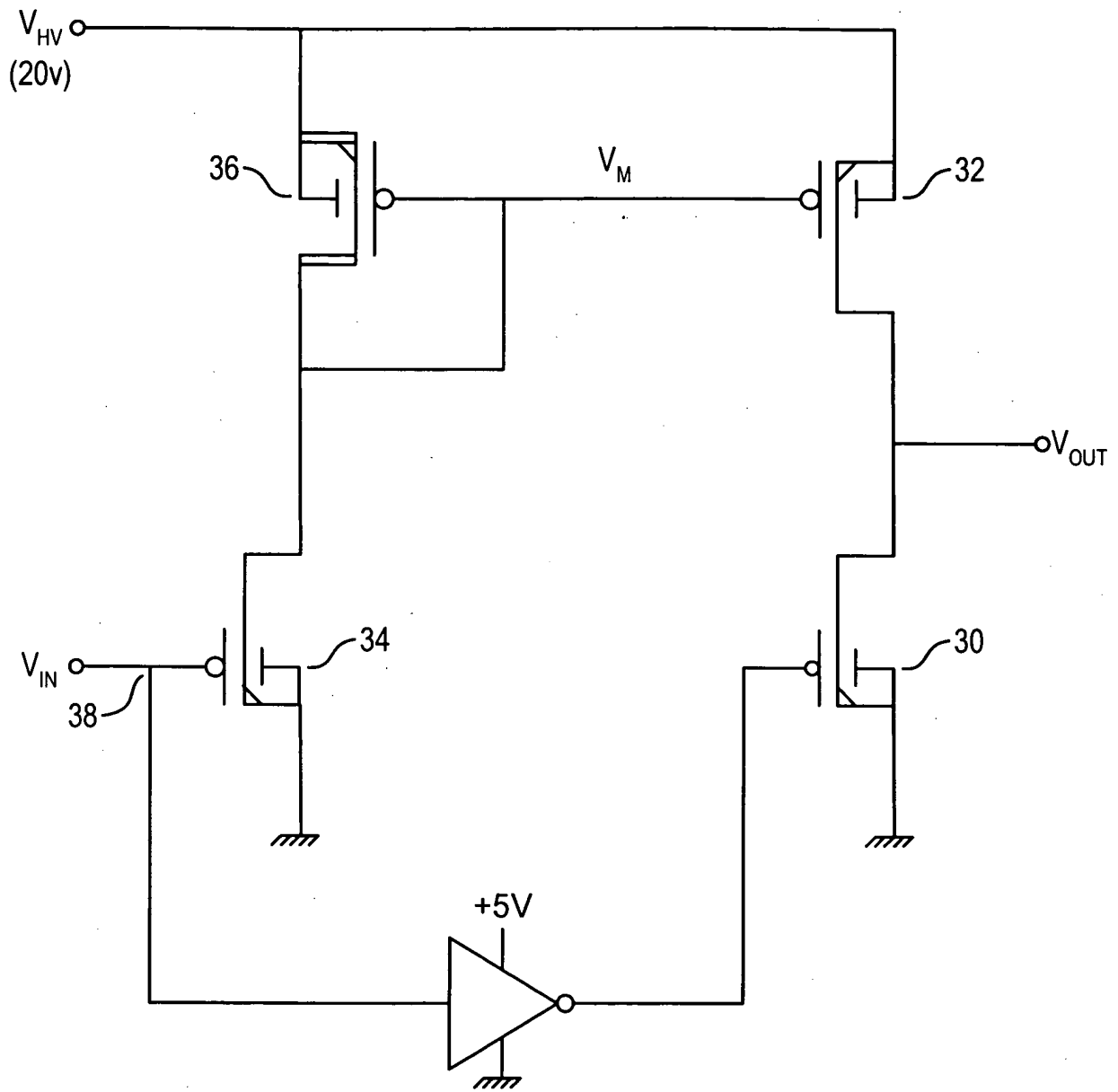
(d) HV NDMOS



(e) HV PDMOS

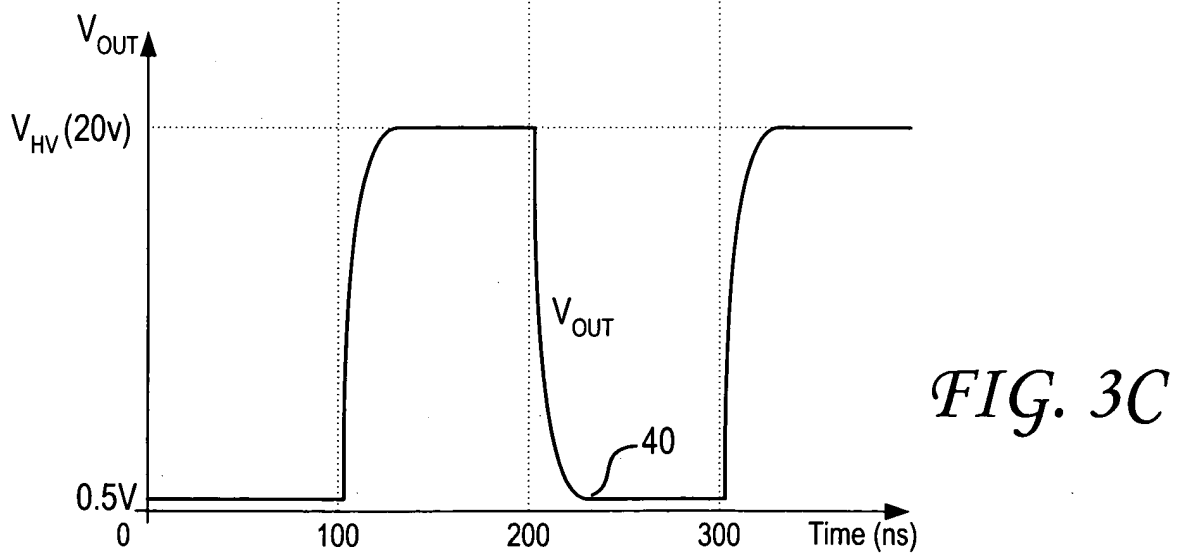
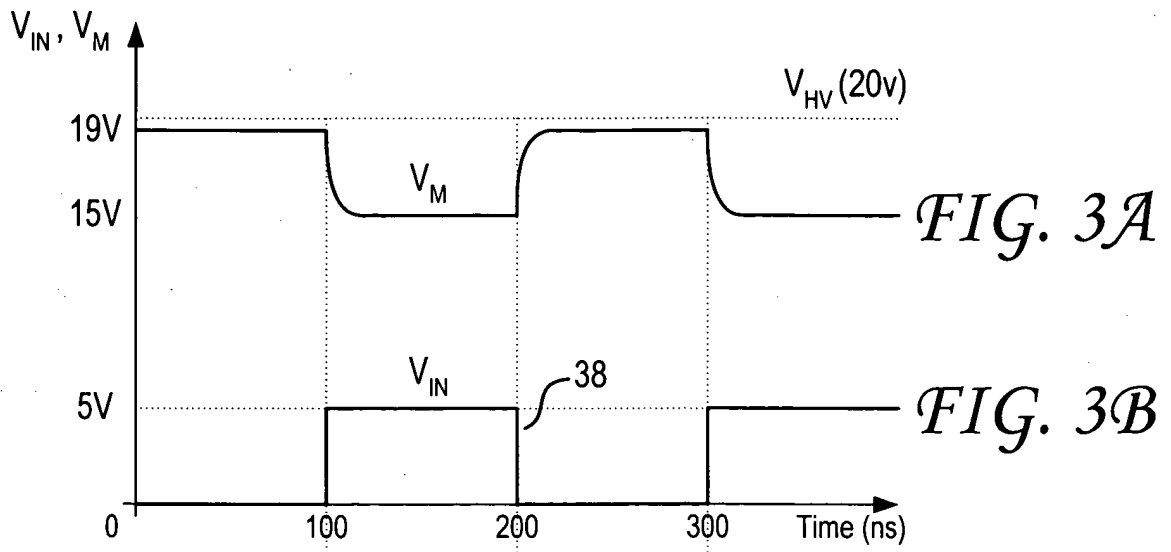
PRIOR ART

FIG. 1

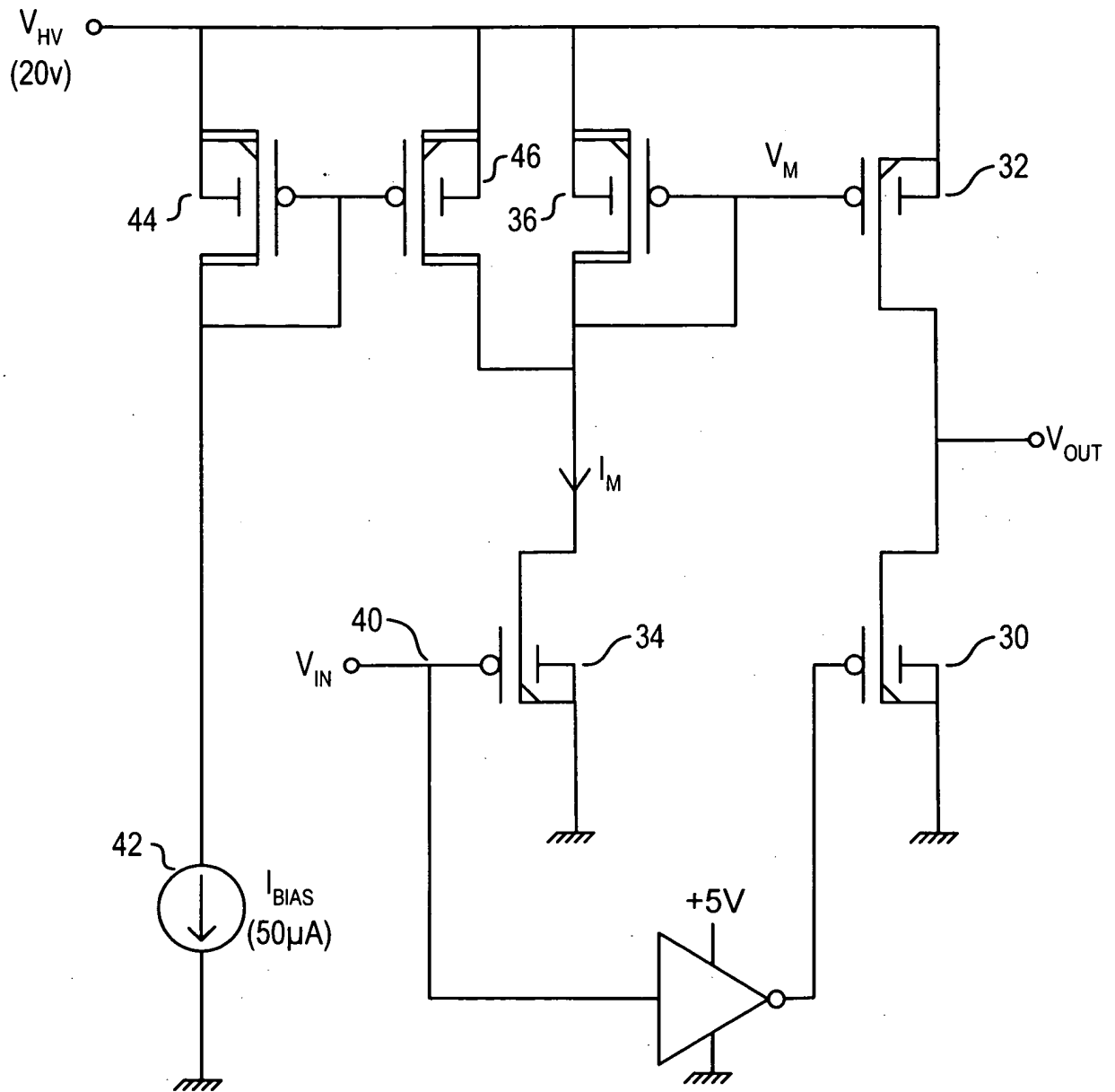


PRIOR ART

FIG. 2

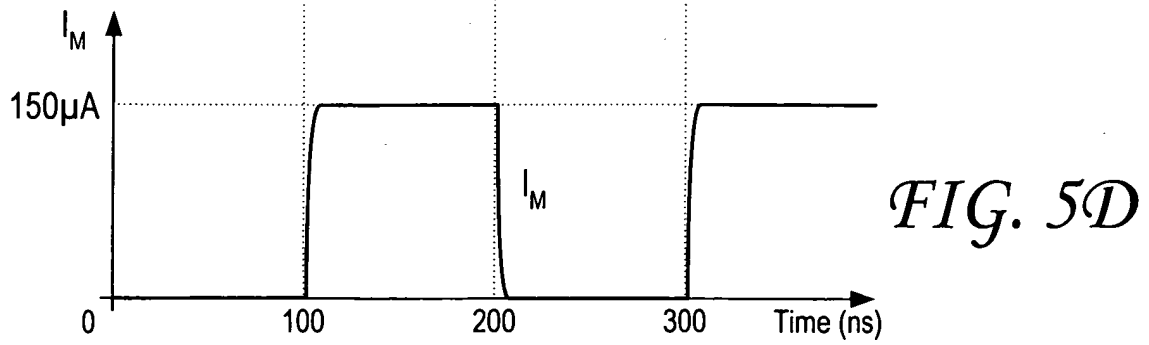
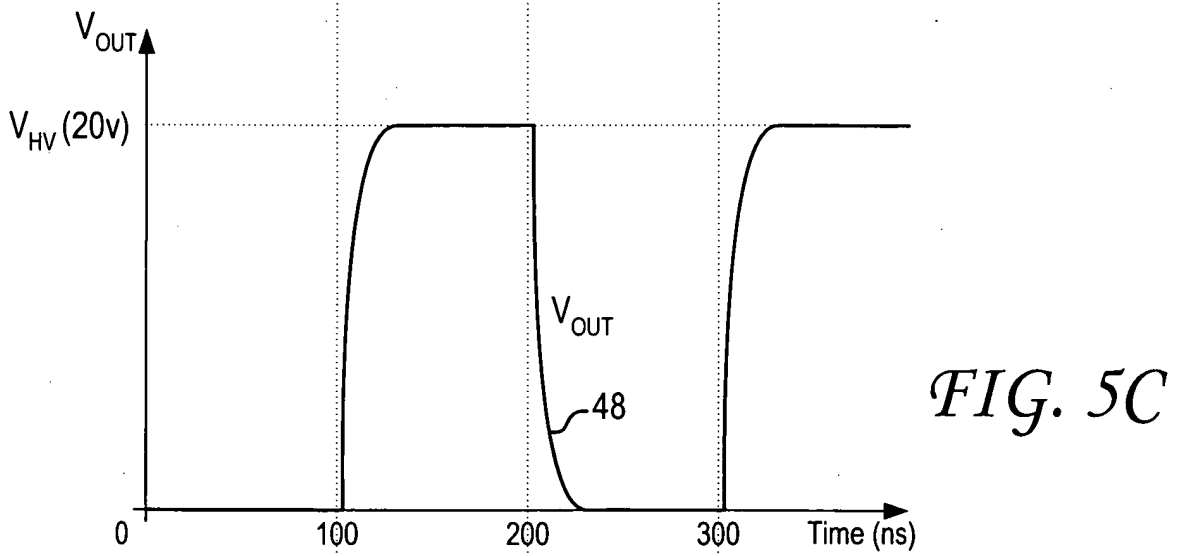
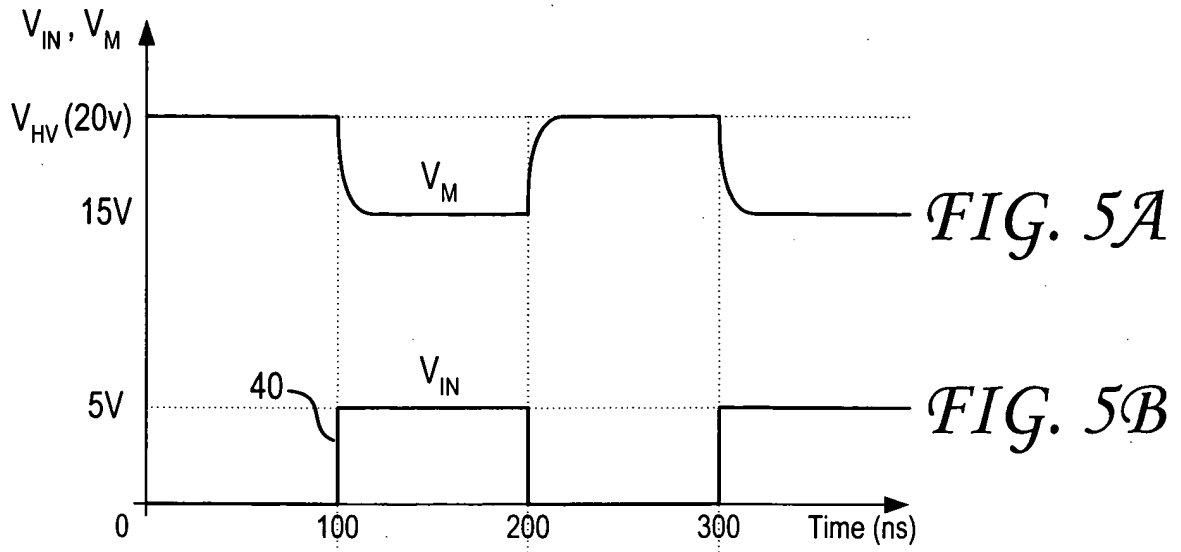


PRIOR ART

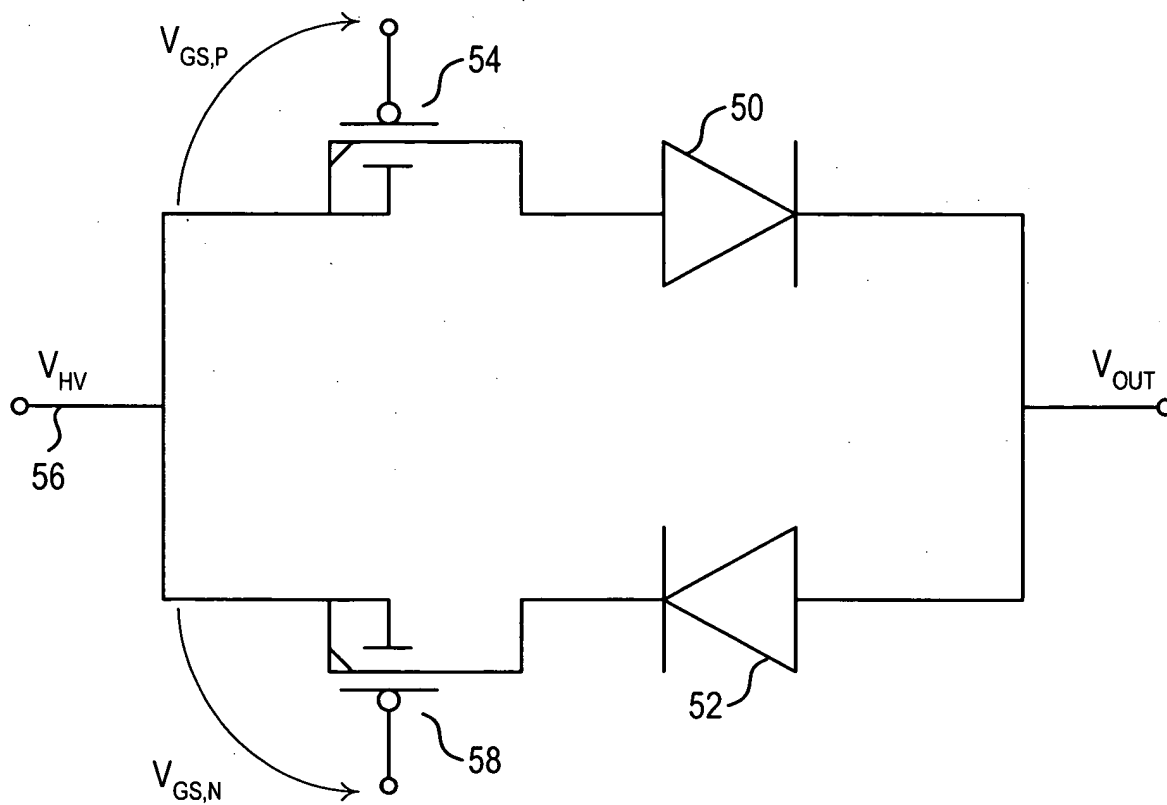


PRIOR ART

FIG. 4



PRIOR ART



PRIOR ART

FIG. 6

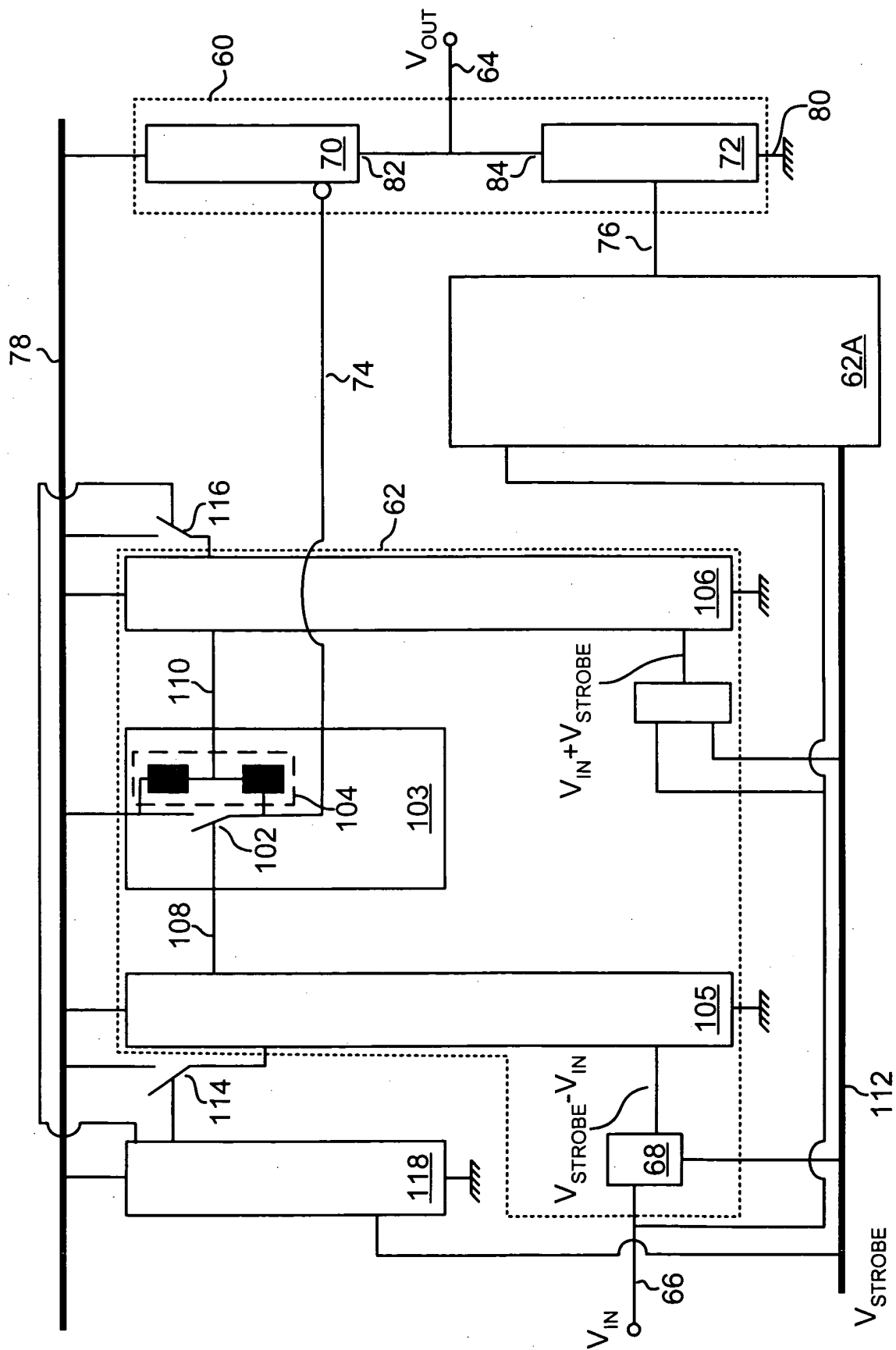


FIG. 7

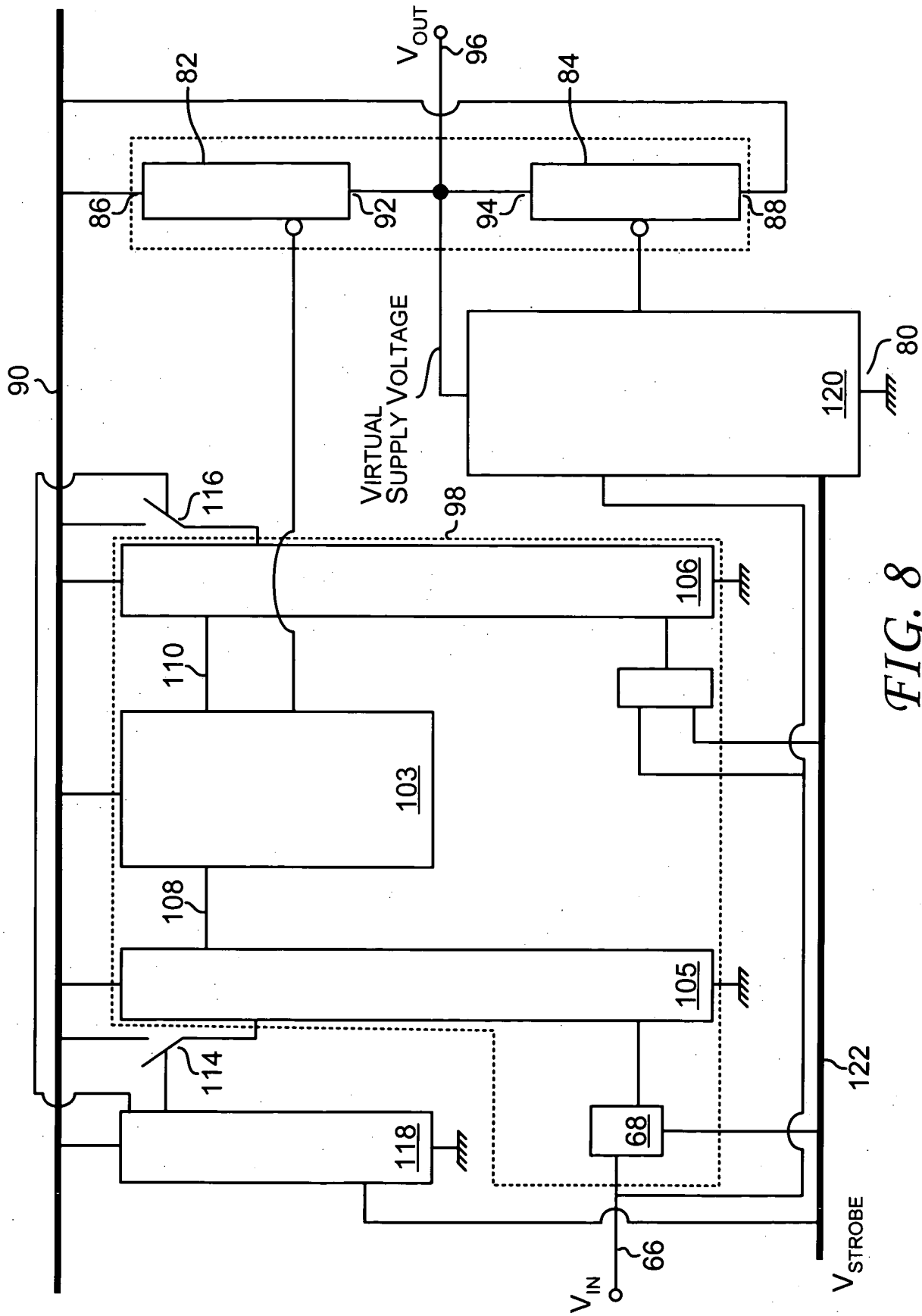


FIG. 8

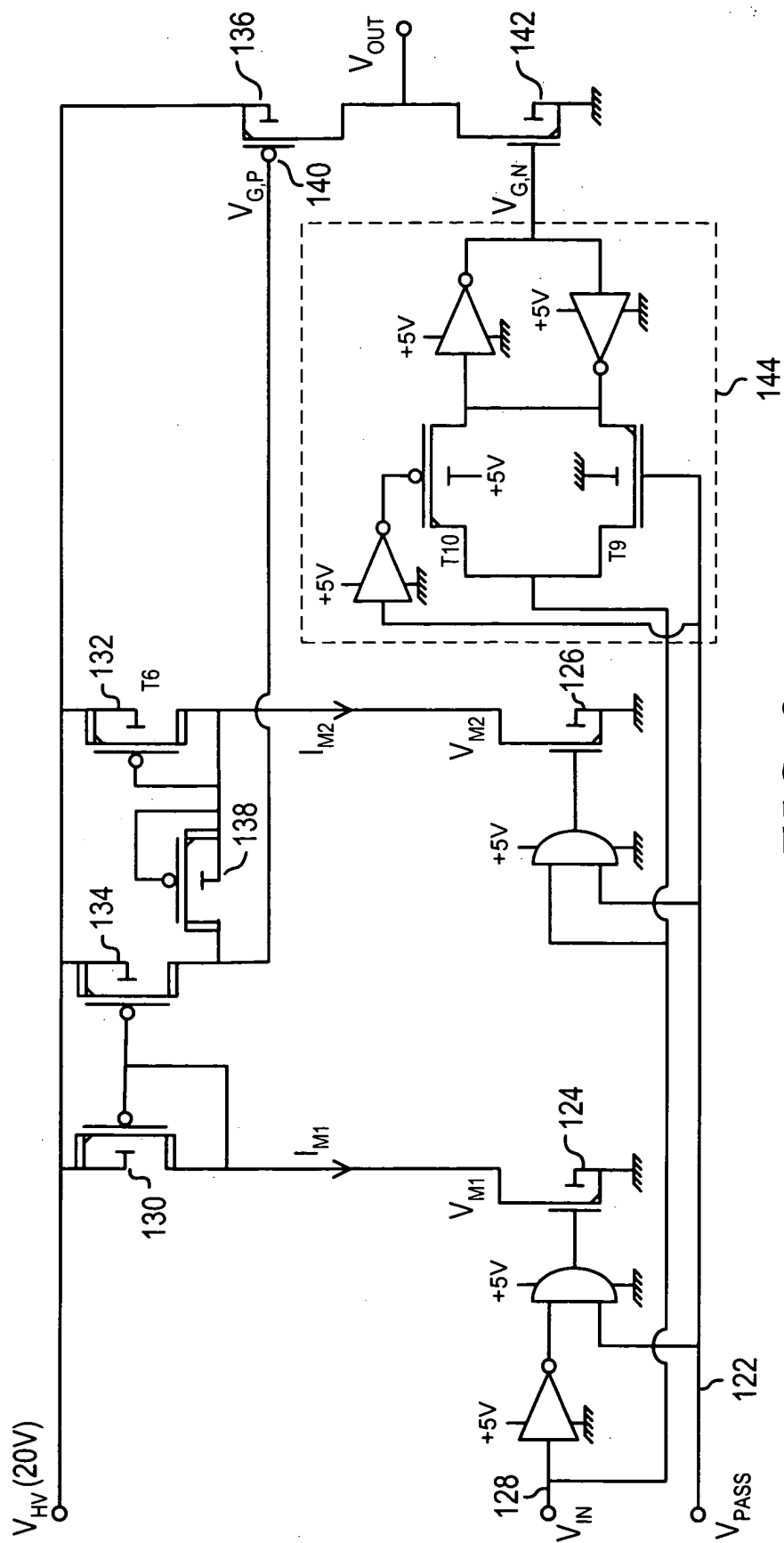
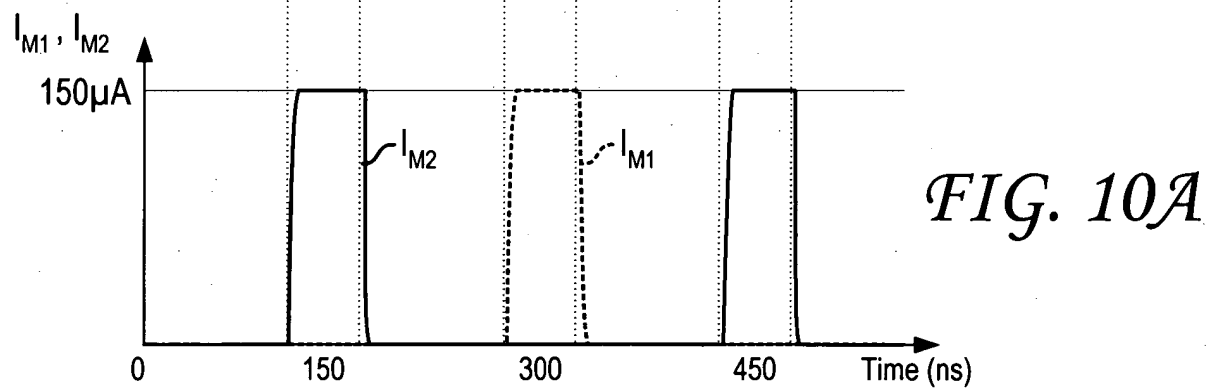
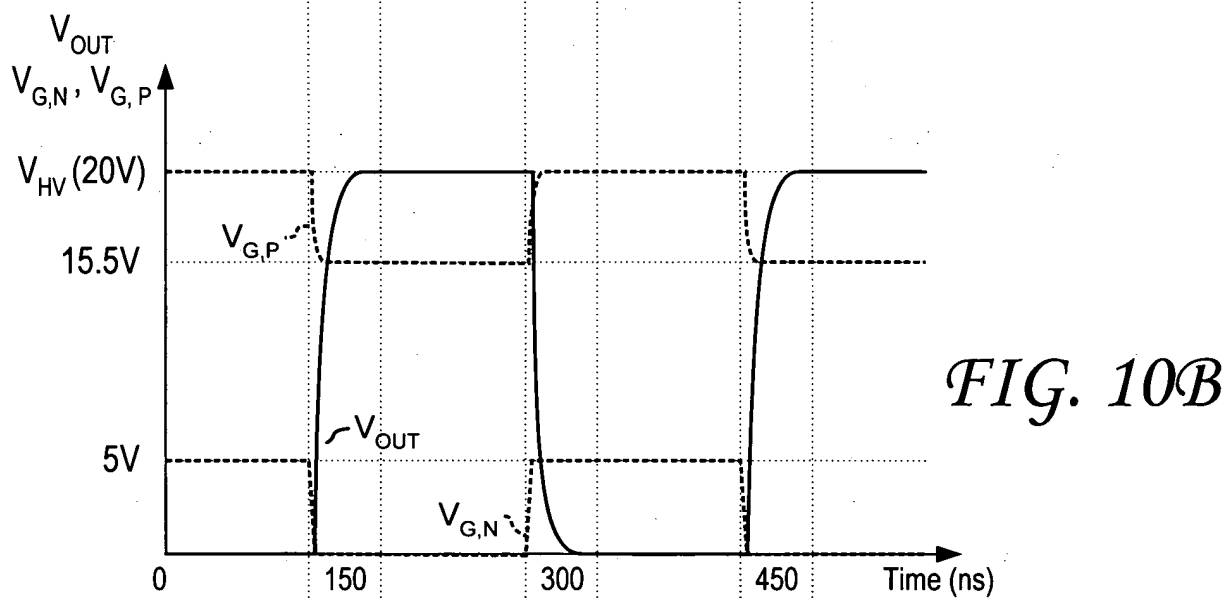
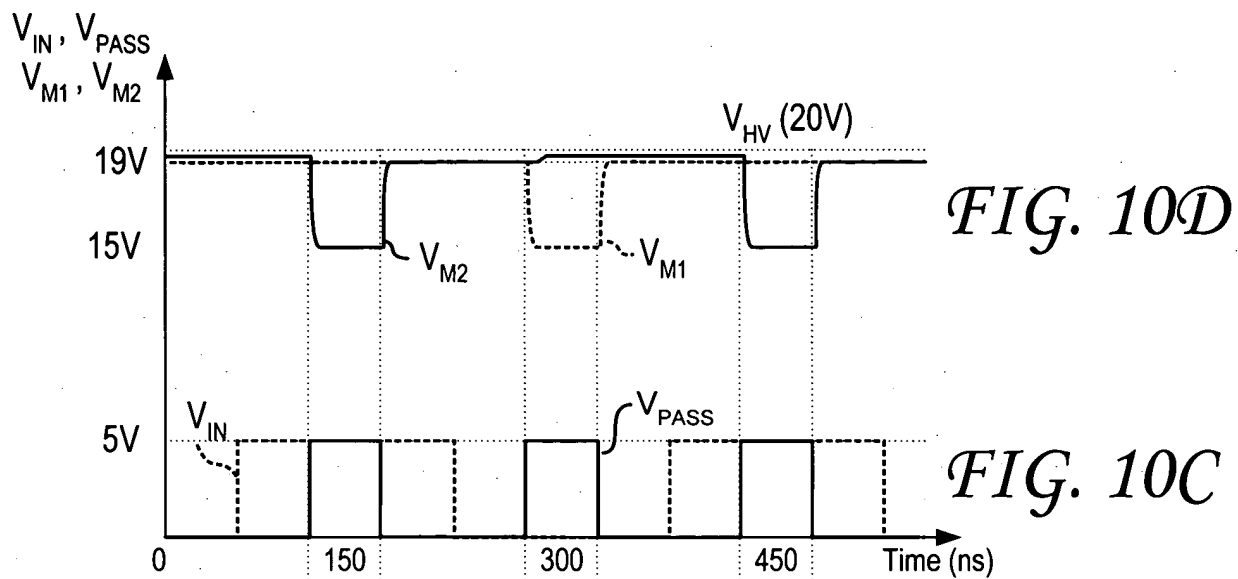


FIG. 9

(10/25)



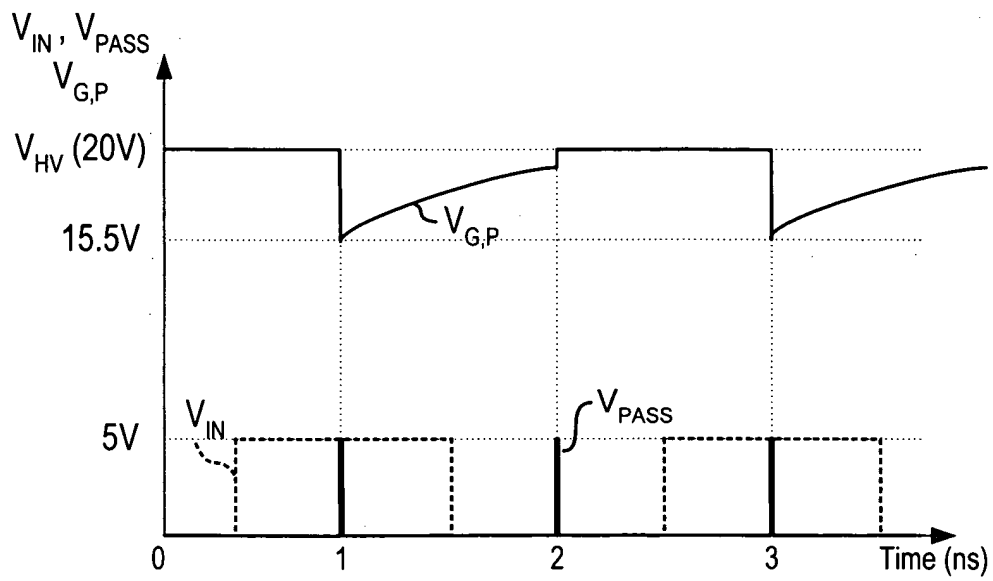
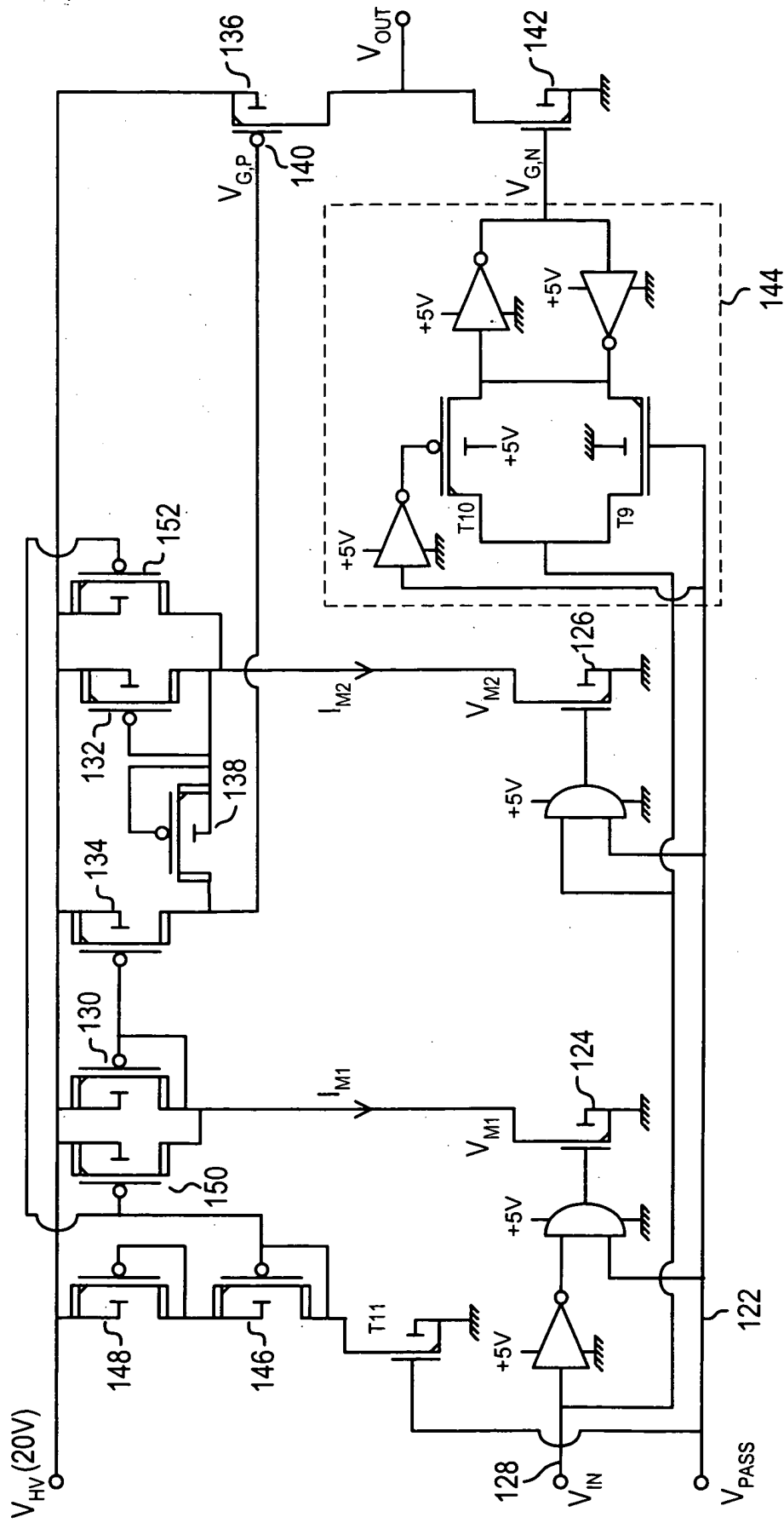
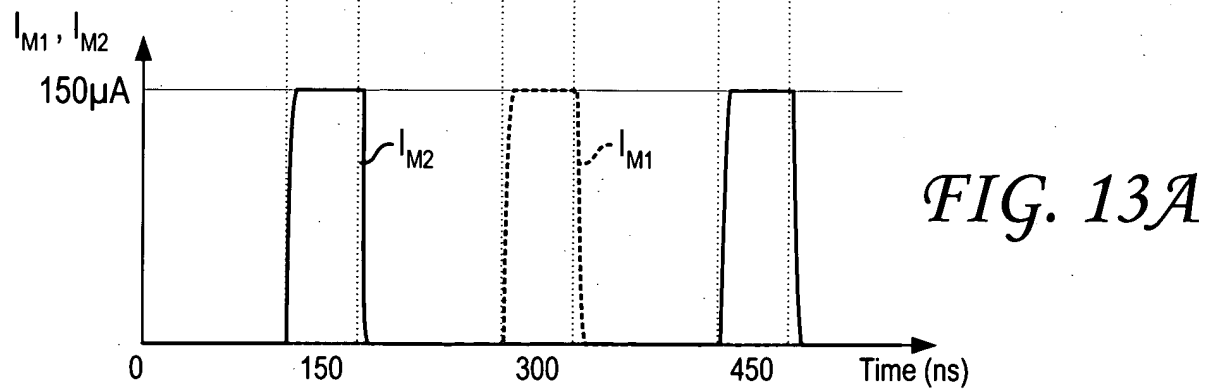
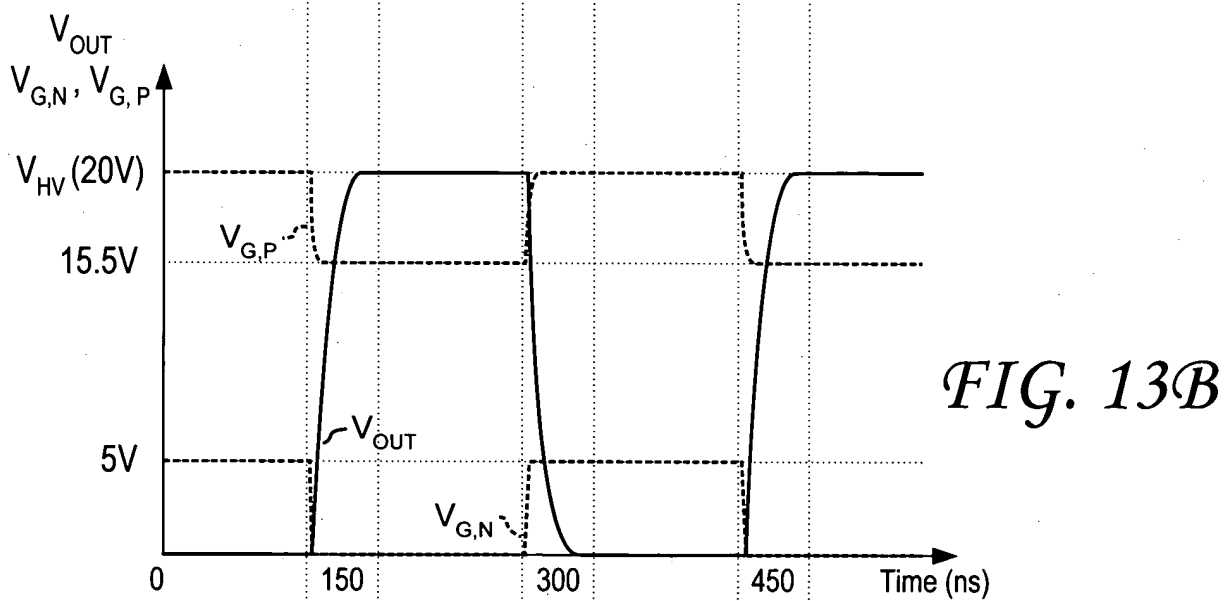
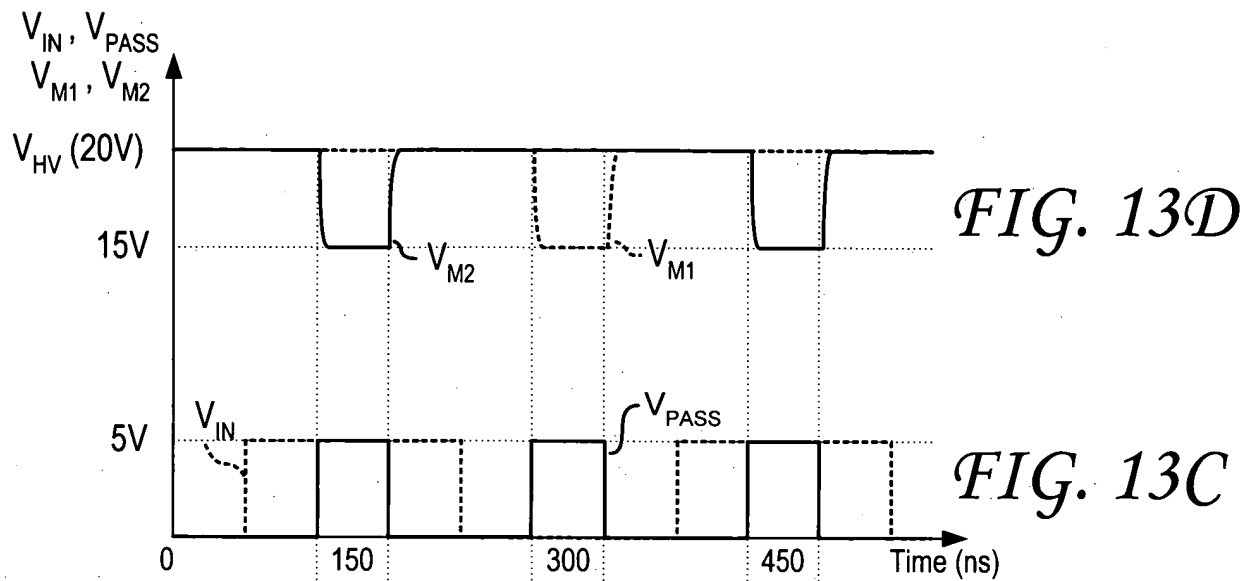


FIG. 11



IMPROVED DYNAMICALLY CONTROLLED HIGH-VOLTAGE LEVEL-SHIFTER WITH EXTREMELY LOW POWER CONSUMPTION

FIG. 12



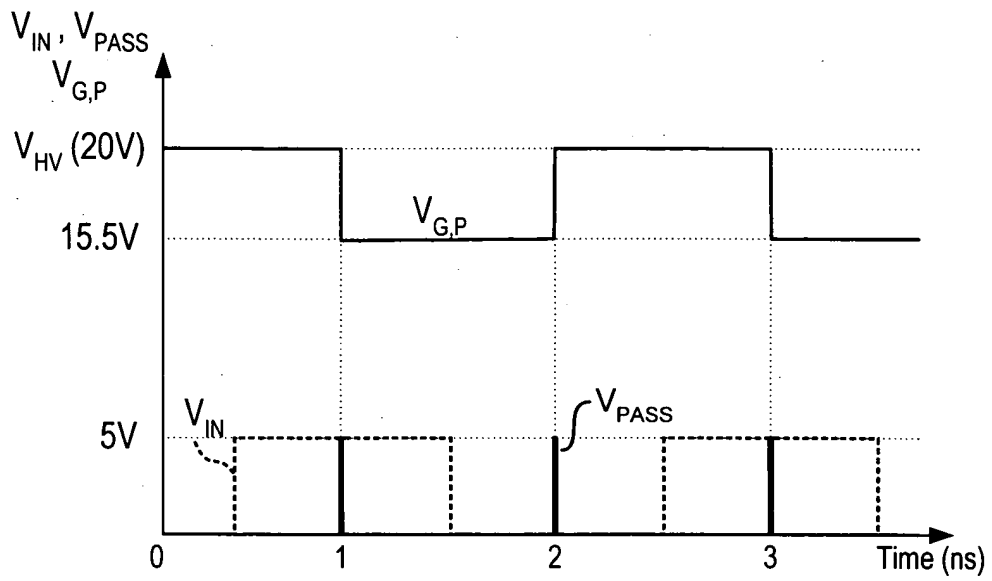


FIG. 14

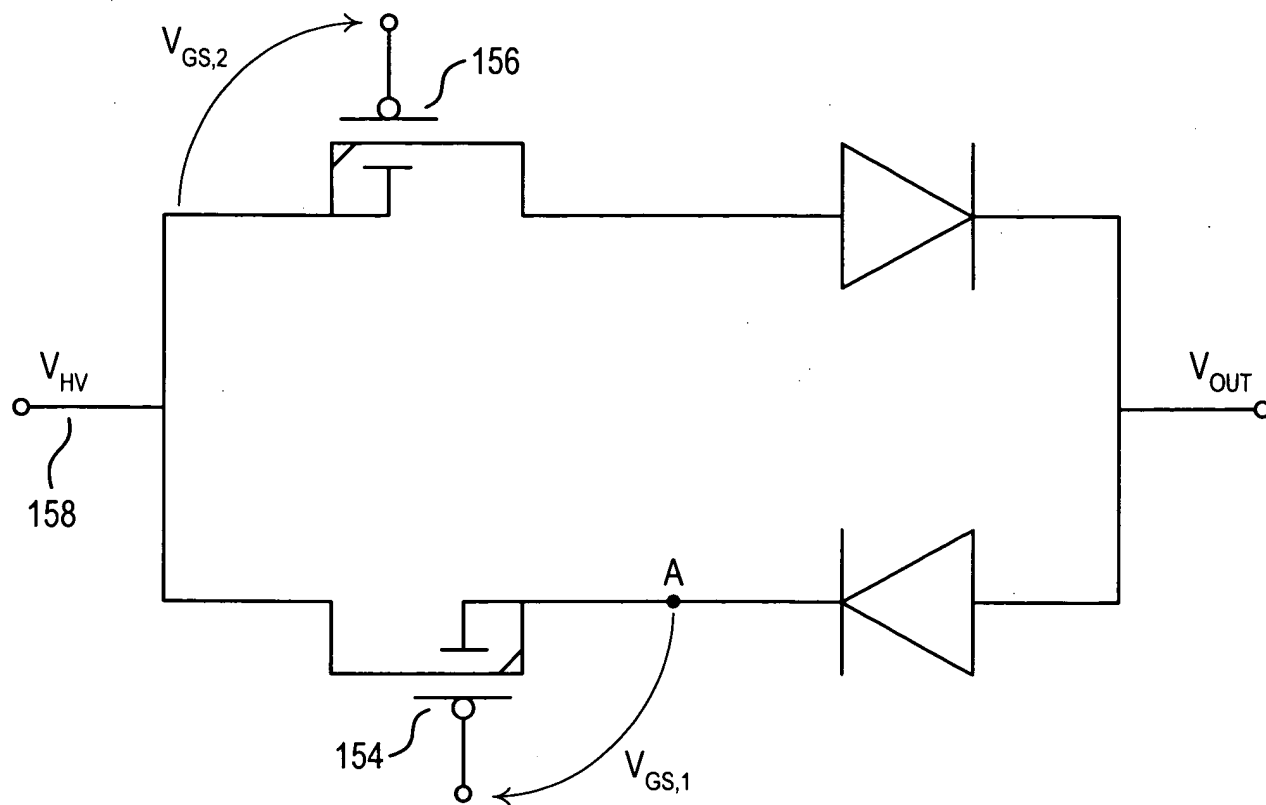


FIG. 15

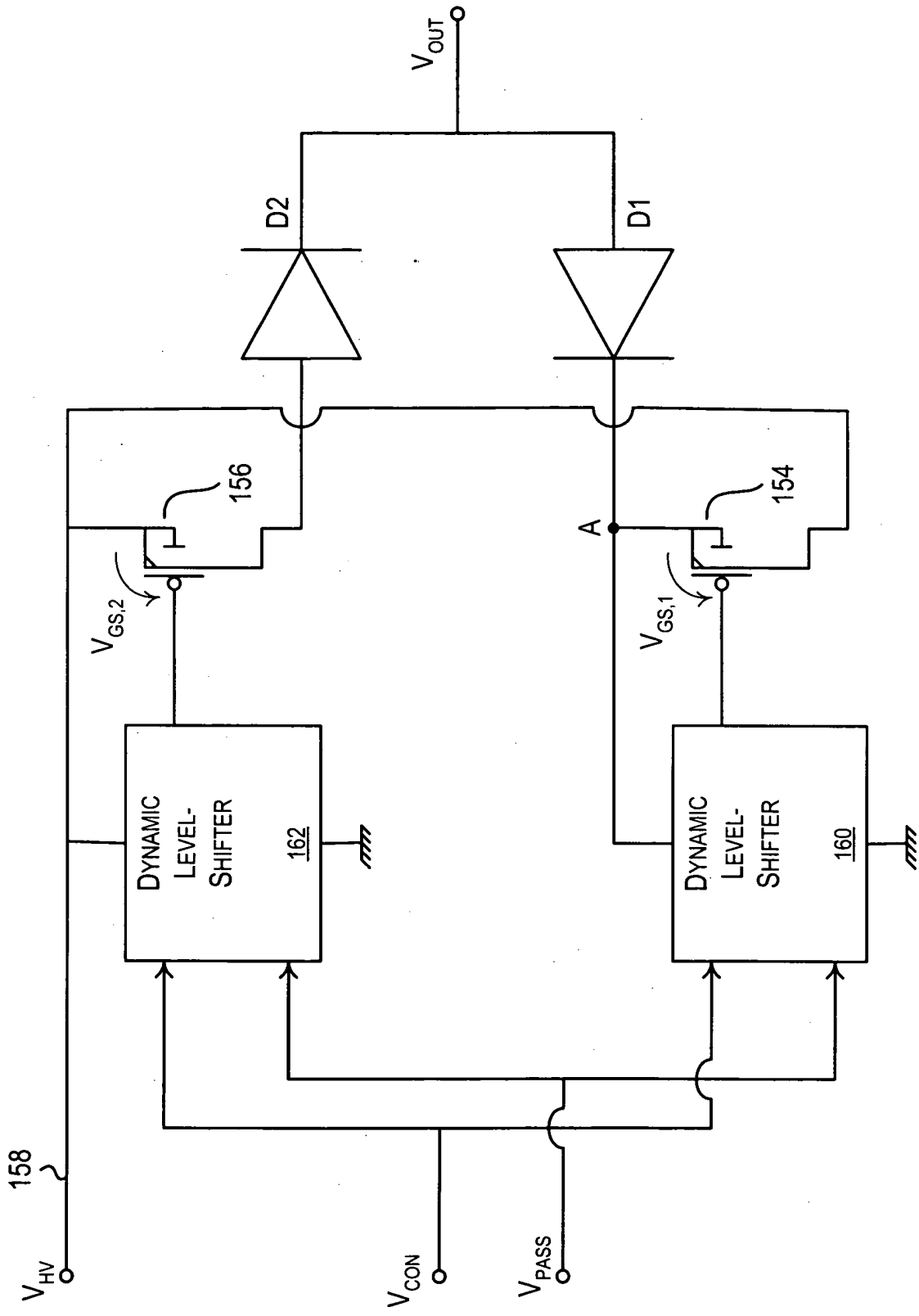


FIG. 16

(17/25)

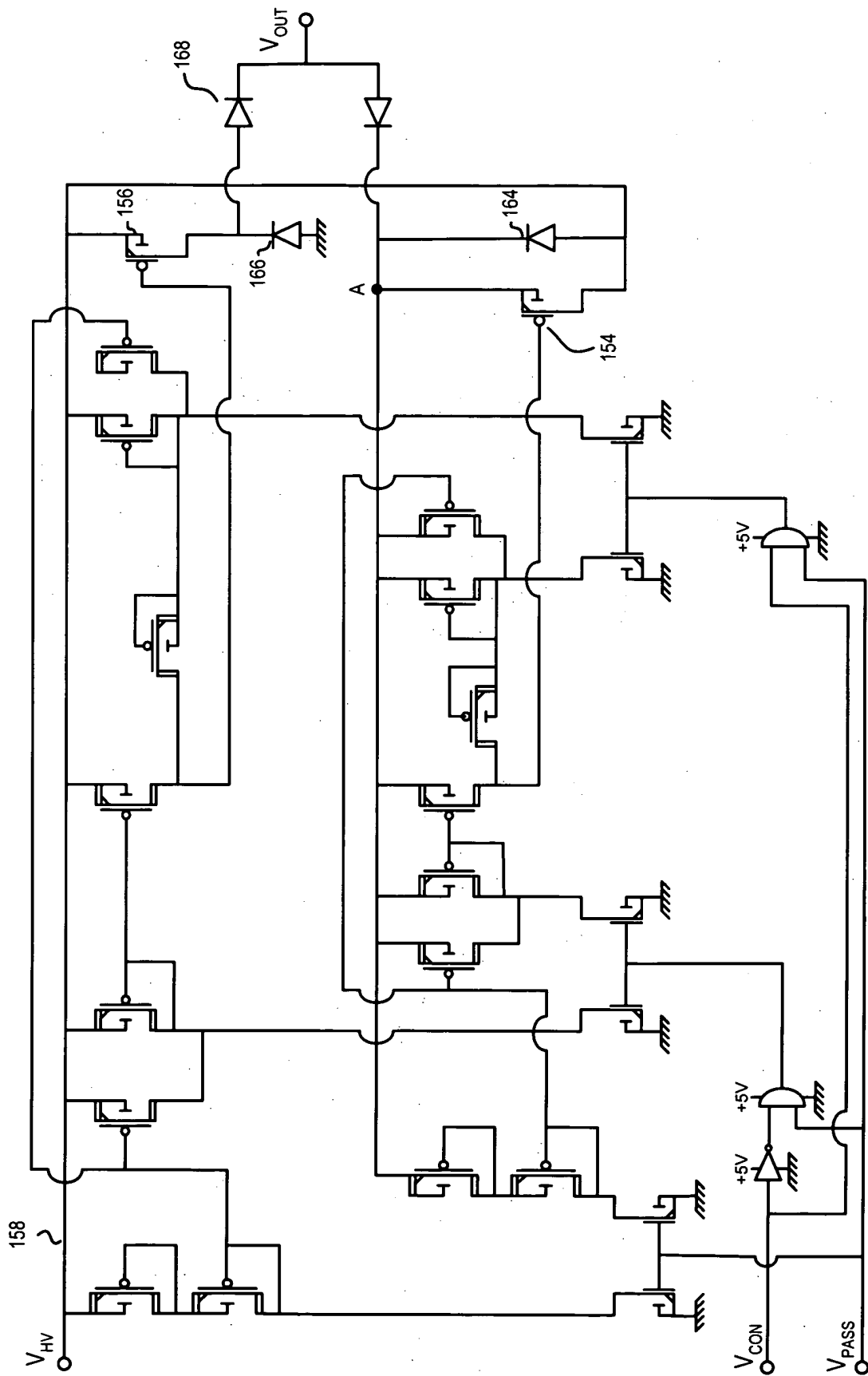


FIG. 17

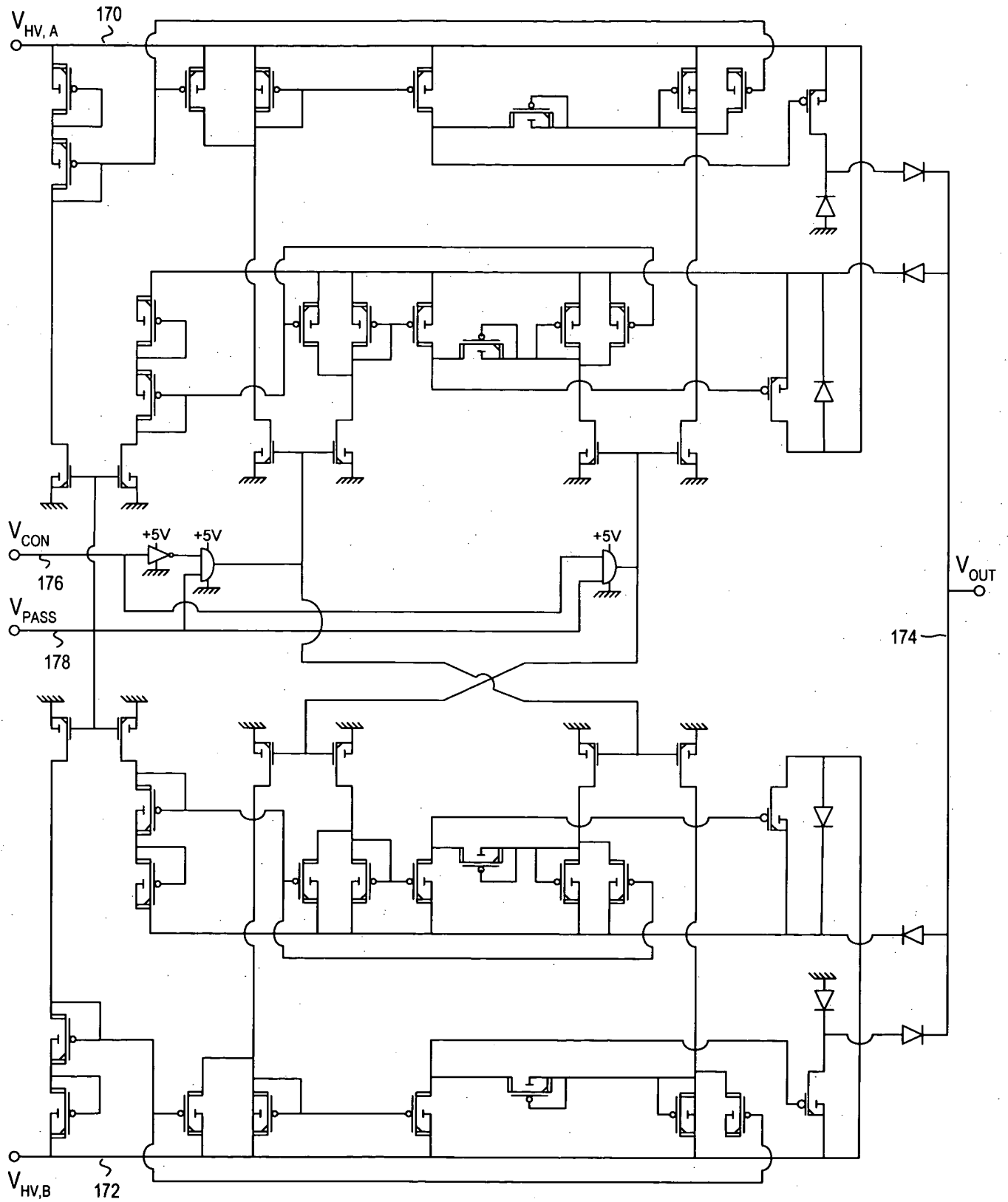


FIG. 18

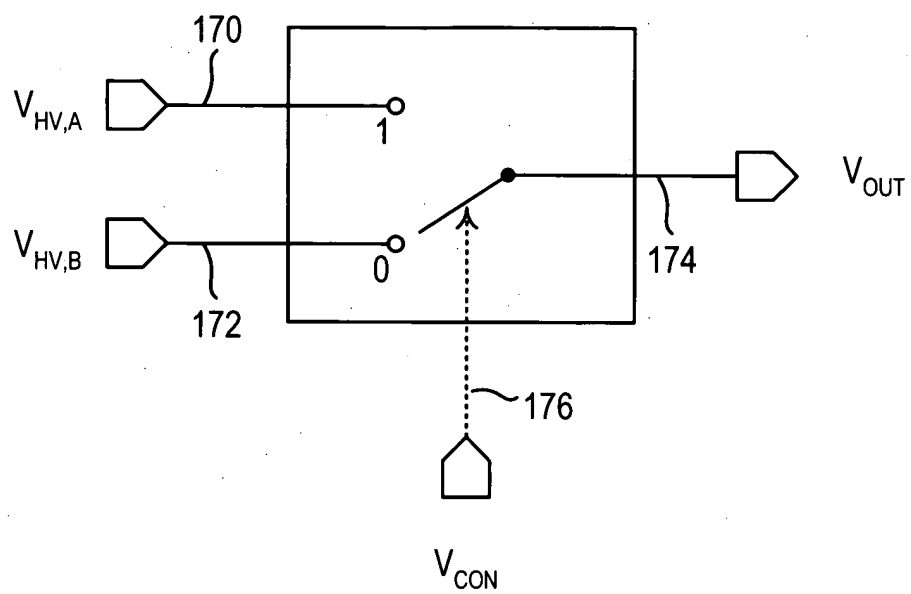
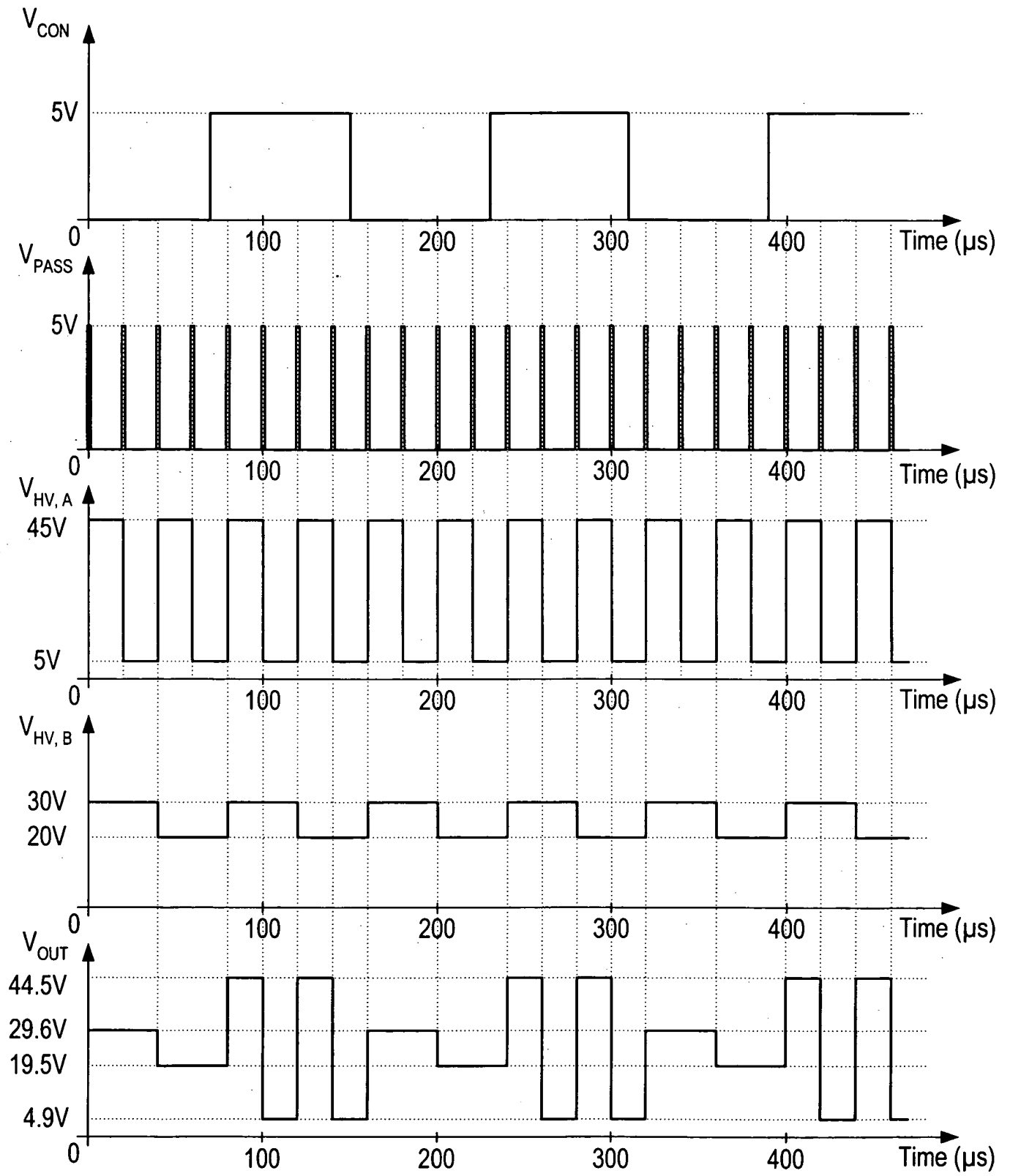


FIG. 19

*FIG. 20*

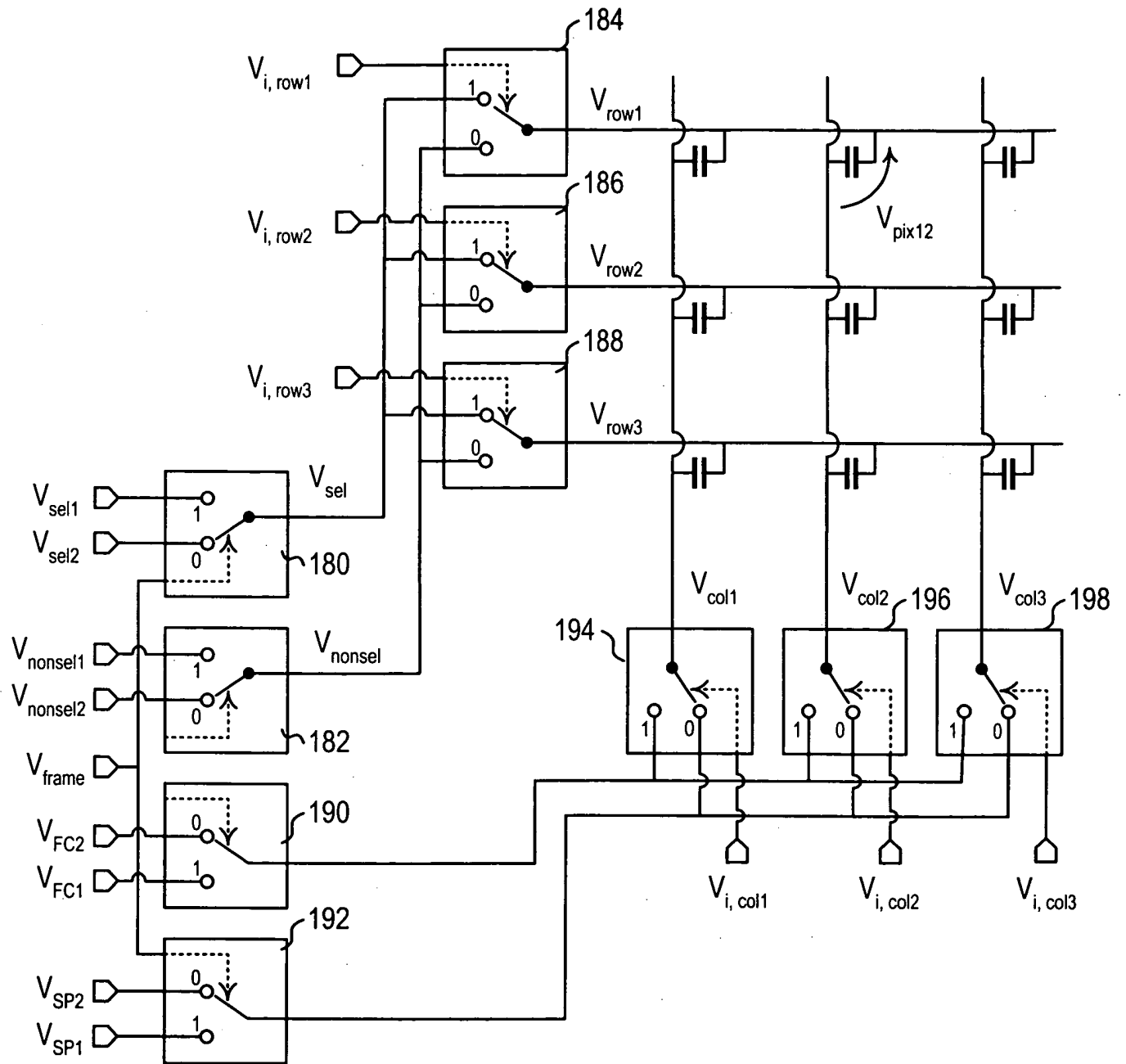
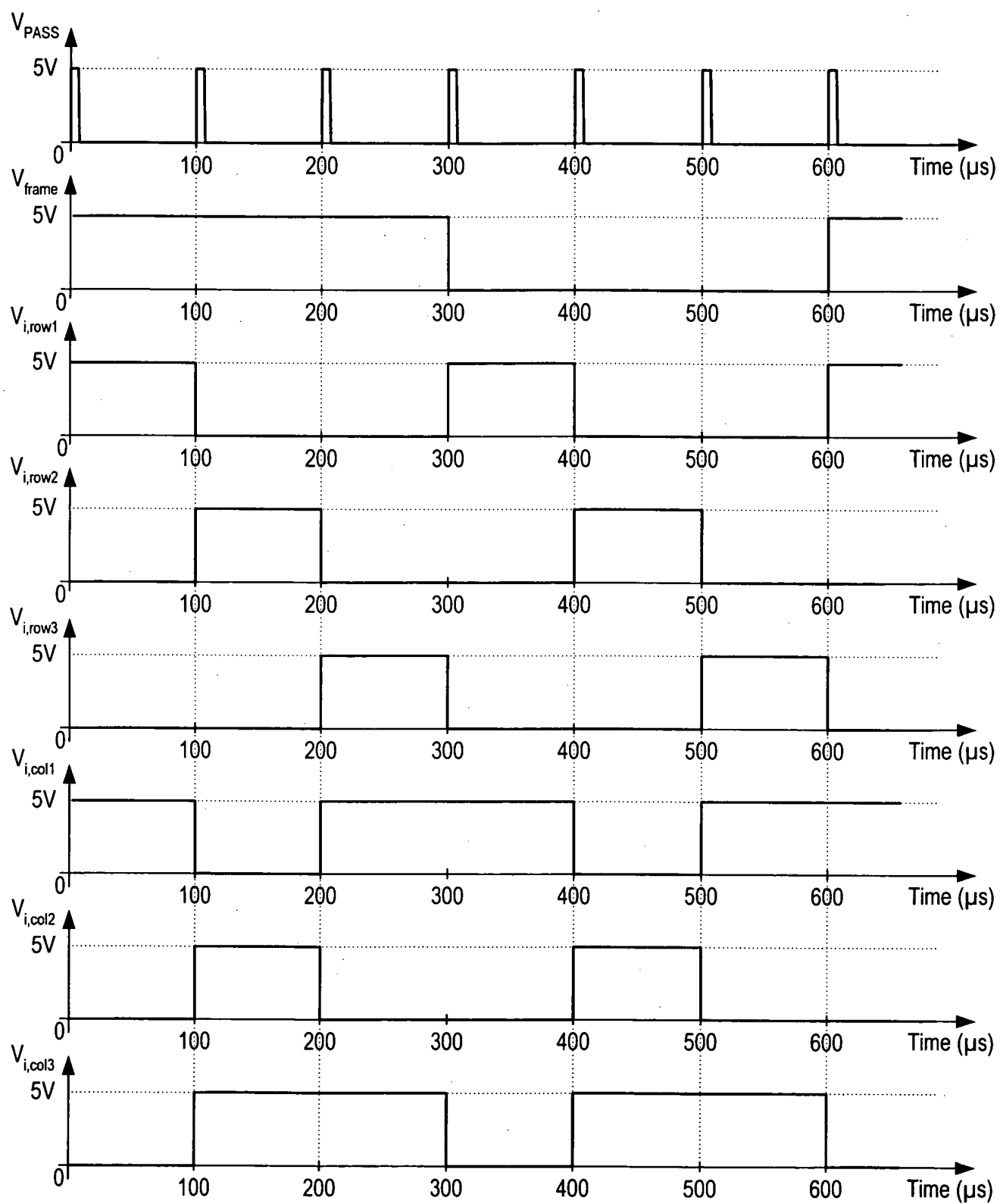


FIG. 21

FC	SP	SP
SP	FC	FC
FC	SP	FC

FIG. 22

*FIG. 23A*

(24/25)

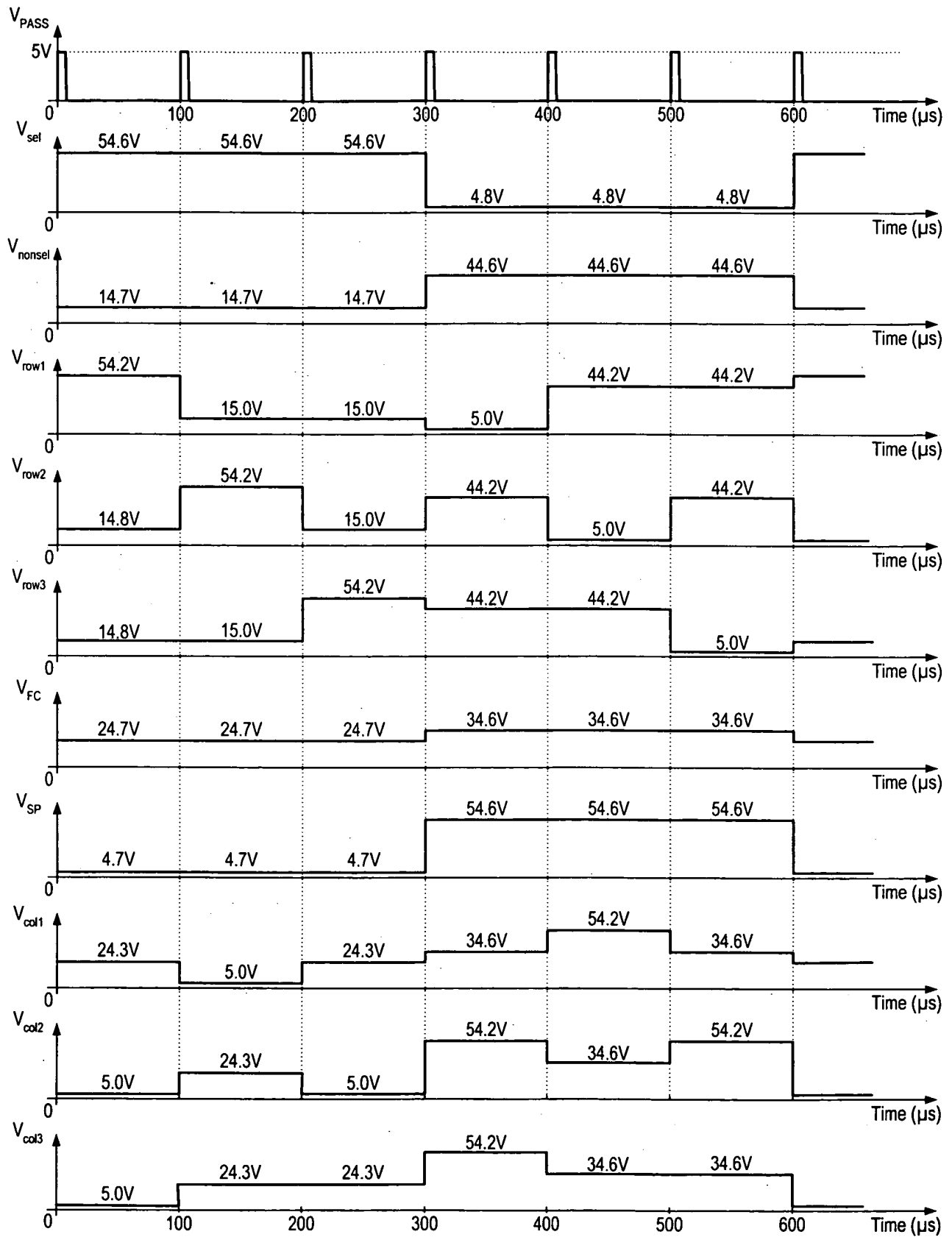


FIG. 23B

(25/25)

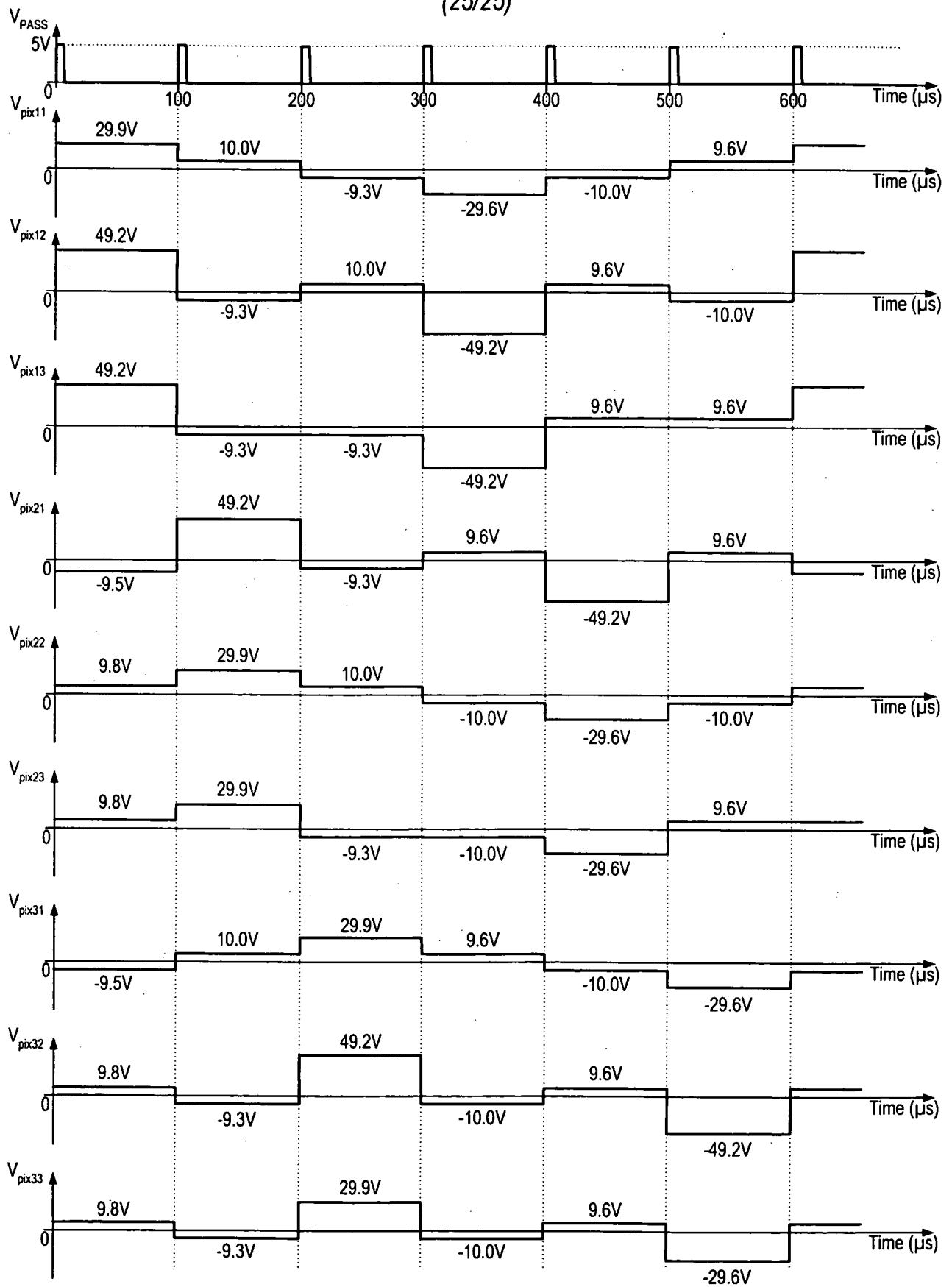


FIG. 23C